

## ABSTRACT OF THE DISCLOSURE

The present invention advantageously provides a substantially planarized semiconductor topography and method for making the same by forming a plurality of dummy features in a dielectric layer between a relatively wide interconnect and a series of relatively narrow interconnect. According to an embodiment, a plurality of laterally spaced dummy trenches are first etched in the dielectric layer between a relatively wide trench and a series of relatively narrow trenches. The dummy trenches, the wide trench, and the narrow trenches are filled with a conductive material, e.g., a metal. The conductive material is deposited to a level spaced above the upper surface of the dielectric layer. The surface of the conductive material is then polished to a level substantially coplanar with that of the upper surface of the dielectric layer. Advantageously, the polish rate of the conductive material above the dummy trenches and the wide and narrow trenches is substantially uniform. In this manner, dummy conductors spaced apart by dielectric protrusions are formed exclusively in the dummy trenches, and interconnect are formed exclusively in the narrow and wide trenches. The topological surface of the resulting interconnect level is substantially void of surface disparity.

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